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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
NGUYEN, THAN VINH	
ART UNIT	**PAPER NUMBER**
2187	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/817,212	KLEIMAN ET AL.	
	Examiner	Art Unit	
	Than Nguyen	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16 and 39-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16 and 39-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/7/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-16,39-41 are pending.

2. The IDS, filed 7/7/05, has been considered.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-16,39,40 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. As to claim 1, Applicant claims "**identifying blocks within the plurality of blocks for use** by the I/O operations as **to substantially maximize chain lengths of reads for calculation of parity and of writes for data write operations thereof while substantially minimizing** cost of calculation of parity, wherein the block identification comprises the steps of examining all the I/O operations, **selecting a method** for parity calculation **which substantially minimizes** cost of the parity calculation for the I/O operations, and responsive to the block layout information and the parity calculation method selection, identifying the blocks within the plurality of blocks for use by the I/O operations." Applicant claims identifying blocks to maximize chain lengths but does not provide the steps needed to maximize the chain lengths. The limitations of "to substantially maximize chain lengths of reads for calculation of parity and of writes for data write operations thereof while substantially minimizing cost of calculation of parity" lengths" and "which substantially minimizes cost of the parity calculation for the I/O operations" are

only expected results, not an actual functional steps to achieve the results. Without specific steps to achieve those results, one of ordinary skills cannot make and/or use the invention, as claimed. For purposes of examination, the Examiner can only interpret above limitations as identifying blocks within the plurality of blocks for use by the I/O operations and a method for parity calculation. The expected results of performing such steps are that the chain lengths are maximized and the parity calculation is minimized.

6. Claims 2,5,6,7,8,9,16,39,40 are similar to claim 1 in that they also claim a result of an operation/step without identifying the necessary steps required to achieve that result. These claims are also rejected on the same grounds as claim 1. For examination purposes, the limitations associated with "maximizing" or "minimizing" are treated as expected results and not given weight.

7. Claims 3-15 are also rejected for incorporating the error of the parent claim 2.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1-16,39-41 are rejected under 35 U.S.C. 102(e) as being anticipated by Corbett (US 6,993,701).

As to claim 1:

10. Corbett teaches a method for managing storage of data in a plurality of storage devices, each storage device comprising a plurality of blocks for storing data, the method comprising the steps of: generating block layout information in a file system layer of the storage operating system by determining which blocks within the plurality of blocks are allocated for storing data and which are unallocated and transferring the block layout information from the file system layer to a RAID layer of the storage operating system (forming/gathering blocks to be written in stripe to minimize parity calculation; 5/50-67); and responsive to the block layout information, the RAID layer controlling the execution of I/O operations by identifying blocks within the plurality of blocks for use by the I/O operations (store blocks contiguously; 5/53-65; 9/4-10) [*so as to substantially maximize chain lengths of reads for calculation of parity and of writes for data write operations thereof while substantially minimizing cost of calculation of parity*], wherein the block identification comprises the steps of examining all the I/O operations, selecting a method for parity calculation [*which substantially minimizes cost of the parity calculation for the I/O operations*], and responsive to the block layout information and the parity calculation method selection, identifying the blocks within the plurality of blocks for use by the I/O operations (calculate parity with subtraction or recalculation method; 9/20-25; 6/30-35; 12/53-60) . It should also be noted that Hitz also teaches selecting between subtraction and recalculation parity calculation methods (US 2003/0037281; 0043-0045, 0114-0115).

As to claim 2:

11. Corbett teaches a method for managing storage of data in a plurality of storage devices, each comprising a plurality of storage blocks, the method comprising the steps of: generating block layout information (forming/gathering blocks to be written in stripe to minimize parity calculation; 5/50-67); and in response to the block layout information, controlling the execution of an I/O operation by identifying storage blocks for use by the I/O operation *[so as to substantially minimize cost of calculation of error correction parameters across a stripe]* (store blocks contiguously; 5/53-65; 9/4-10; calculate parity with subtraction or recalculation method; 9/20-25; 6/30-35; 12/53-60).

As to claim 3:

12. Corbett teaches the calculation of error correction parameters comprises the calculation of parity (calculate parity with subtraction or recalculation method; 9/20-25; 6/30-35; 12/53-60).

As to claim 4:

13. Corbett teaches selecting a parity calculation operation from a group consisting of a subtraction method and a parity re-calculation method (calculate parity with subtraction or recalculation method; 9/20-25; 6/30-35; 12/53-60). It should also be noted that Hitz also teaches selecting between subtraction and recalculation parity calculation methods (US 2003/0037281; 0043-0045, 0114-0115).

As to claim 5:

14. Corbett teaches the identification of storage blocks for use in the I/O operation *[substantially maximizes the chain length by substantially maximizing the number of blocks*

having a contiguous physical layout on a storage device] (forming/gathering blocks to be written in stripe to minimize parity calculation; 5/50-67; storing blocks contiguously; 5/53-65; 9/4-10).

As to claim 6:

15. Corbett teaches the step of identifying storage blocks for use in the I/O operation *[so as to substantially maximize the chain length by substantially maximizing the number of blocks having sequential VBN's associated with the storage blocks]* (forming/gathering blocks to be written in stripe to minimize parity calculation; 5/50-67; storing blocks contiguously; 5/53-65; 9/4-10).

As to claim 7:

16. Corbett teaches the step of identifying storage blocks for use in the I/O operation *[so as to substantially maximize the chain length by substantially maximizing the locality of the blocks of a storage device].*

As to claim 8:

17. Corbett teaches the execution controlling step comprises the steps of: examining blocks to which data is to be written prior to write operations; selecting one of a plurality of parity calculation methodologies including a first methodology comprising *[minimizing the number of blocks read, and a second methodology comprising maximizing chain lengths of blocks read for the parity calculation]* (calculate parity with subtraction or recalculation method; 9/20-25; 6/30-35; 12/53-60). It should also be noted that Hitz also teaches selecting between subtraction and recalculation parity calculation methods (US 2003/0037281; 0043-0045, 0114-0115).

18. As to claim 9

19. Corbett teaches implementing the selection responsive to the block layout information (forming/gathering blocks to be written in stripe to minimize parity calculation; 5/50-67); and wherein, if the selection constitutes substantially minimizing the number of read blocks (storing blocks contiguously; 5/53-65; 9/4-10), determining on a stripe-by-stripe basis whether to calculate parity based on a subtraction method or a recalculation method, performing any appropriate read operations to support the method selected, and calculating parity responsive to the read blocks and the data to be written; and wherein, if the selection constitutes substantially maximizing chain lengths of blocks read, deciding which storage blocks to read *[to substantially maximize chain length while substantially minimizing the number of storage blocks read to support either a subtraction method or a recalculation method],* performing read operations on the blocks to be read, and calculating parity responsive to the read blocks and the data to be written (calculate parity with subtraction or recalculation method; 9/20-25; 6/30-35; 12/53-60). It should also be noted that Hitz also teaches selecting between subtraction and recalculation parity calculation methods (US 2003/0037281; 0043-0045, 0114-0115).

As to claim 10:

20. Corbett teaches the identification of storage blocks is based at least in part on an available resource (available resources/devices 5/53-55).

As to claim 11:

21. Corbett teaches transmitting the block layout information from a file system layer to a RAID layer (formed stripes on RAID level; 5/57-66).

As to claim 12:

22. Corbett teaches generating the block layout information based on available resources (forming stripe blocks; 5/53-6/40).

As to claim 13:

23. Corbett teaches wherein the I/O operation is one of a plurality of I/O operations and one of the plurality of I/O operations is a read operation (read/write operations; 3/1-5; 5/43-45; 9/59-60).

As to claim 14:

Corbett teaches the chain length is a chain length of a read operation for calculation of parity (calculate parity; 9/18-35).

As to claim 15:

Corbett teaches the chain length is a chain length for a write operation for the data ((calculate parity; 9/18-35).

As to claim 16:

24. Corbett teaches a method for managing storage of data in a storage system comprising a plurality of storage devices each comprising a plurality of storage blocks, the method comprising writing data to predetermined storage blocks across a plurality of stripes and to predetermined storage blocks within each storage device *[so as to substantially maximize chain length of storage blocks within each storage device while substantially minimizing cost of calculation of*

error correction parameters across each stripe of the plurality of stripes] (forming/gathering blocks to be written in stripe to minimize parity calculation; 5/50-67).

As to claim 39:

25. Corbett teaches a storage system comprising: a plurality of storage devices each comprising: a plurality of storage blocks (RAID; Fig. 2); and a storage manager in communication with the plurality of storage devices (adapter 228; 7/53-63), the storage manager writing data to predetermined storage blocks across a plurality of stripes (forming stripes; 8/35-52) and to predetermined storage blocks within each storage device so *[as to substantially maximize chain length of storage blocks within a storage device while substantially minimizing the calculation of error correction parameters across each stripe of the plurality of stripes]* (forming/gathering blocks to be written in stripe to minimize parity calculation; 5/50-67).

As to claim 40:

26. Corbett teaches a system for managing the storage of data, the system comprising: a plurality of storage devices each having a plurality of storage blocks (RAID; Fig. 2); a storage device manager in communication with the plurality of storage blocks (adapter 228; 7/53-63); a block layout information generator in communication with the storage device manager and the plurality of storage blocks (forming stripes; 8/35-52); and an error correction parameter calculator (operating system 600 calculates parity; 8/18-34) in communication with the plurality of storage blocks and the storage device manager, wherein the storage device manager, in response to the block layout information from the block layout information generator, controls the execution of an I/O operation by identifying storage blocks for use by the I/O operation *[so*

as to substantially maximize chain length within the storage device while substantially minimizing the calculation by the error correction parameter calculator of error correction parameters across a stripe] (forming/gathering blocks to be written in stripe to minimize parity calculation; 5/50-67).

As to claim 41:

27. Corbett teaches a method for managing storage of data in storage blocks, the method comprising the steps of: generating block layout information (forming stripes; 8/35-52); dynamically determining a first number of error correction calculations (calculate parity with subtraction or recalculation method; 9/20-25; 6/30-35; 12/53-60); dynamically determining a second number corresponding to a chain length and in response to the block layout information, controlling the execution of an I/O operation by identifying storage blocks for use by the I/O operation so as to have a chain length of the second number within a storage device while performing the first number of calculations of error correction parameters across a stripe (forming/gathering blocks to be written in stripe to minimize parity calculation; 5/50-67).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Than Nguyen whose telephone number is 571-272-4198. The examiner can normally be reached on 8am-3pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Than Nguyen
Primary Examiner
Art Unit 2187